REMARKS

The Invention

The invention is a method of forming a MOS or CMOS device on a silicon substrate. The substrate is prepared, and includes a conductive region of a first type, such as an n-type or p-type conductive region, which has a first device active area therein. Two such regions are prepared, of opposite conductive types, for a CMOS device. A gate electrode is formed on the active area(s). Ions of an opposite conductivity type to that of the conductive region of the first type are implanted into the conductive region of the first type to form a source region and a drain region on opposite sides of the gate electrode. An important feature of the invention is the fabrication of a device using only a single implantation step and a single mask and the deposition of a silicide layer by selective CVD, which does not require further masking. The reduction in implantation and masking steps saves time and reduces the overall cost of the fabrication process. In fact, the method of the invention saves two mask levels during fabrication of a CMOS device, and saves two-ion implantation steps during CMOS fabrication. The silicide layer is formed with only a single, selective CVD process.

The Applied Art

U. S. Patent No. 4,703,551 to Szluk *et al.* describes a method of implantation which requires at least two, and likely three, separate implantation steps. Not only are these multiple implantation steps described in the Specification, the claims require multiple implantation steps. Elimination of any of the doping steps will render any devices formed by the method of the invention inoperative. One implantation step is described as lightly doping, col. 9, lines 30-50,

while another implantation step is described as heavy, col. 5, line 66 - col. 6, lines 14. The light doping step is conducted with too great an ion dose, the ions will leak into the channel, rendering the device inoperative. thus, a multi-step implantation is required by the '551 reference. A tungsten layer is formed, and is stated to be equivalent to a refractory metal silicide layer. Col. 9, lines 61- col. 10, line 7. However, additional masking is required for this process.

U. S. Patent No. 5,757,045 to Tsai *et al.* describes a standard silicide process, and also describes, and requires, multiple masking and implantation steps for each device in the CMOS. Col. 3, line 65 to col. 5, line 22.

U. S. Patent No. 6,069,044 to Wu describes a multi-step, low energy implantation process.

The Claims

Claim 1, as filed recites a single implantation step, which is know to those of ordinary skill in the art to require only a single mask, and selective deposition of silicide. The claim is allowable because all of the references applied by the Examiner require, and are inoperative without, multiple implantation and masking steps.

Claims 2-5 are allowable with their allowable parent claims.

Claim 6 has been amended to further emphasize that the implantation for a MOS device is done in a single step with a single mask, and that the deposition of silicide is done selectively. This differs from the teachings of the applied references, taken separately or alone. The amendment also further distinguishes claim 6 from claim 1, and the "double patenting" rejection should thus be removed, although the claims as filed recited differences believed to be

sufficiently patentably distinct.

Claims 7-10 are allowable with their allowable parent claims.

Claim 11, as filed recites a method of forming a CMOS device, and again, recites only a single implantation step for each of the device active areas, which, as is well know to those of skill in the art, requires only a single masking step. Claim 11 is allowable as filed because the applied reference(s) for each of the 35 U.S.C. § 102 rejection require multiple masking and implantation steps, and the devices constructed according to the references will be inoperative with only a single implantation step.

Claim 13-16 are allowable with their allowable parent claims.

Claim 17 has been amended to further clarify that implantation for each of the device active areas in the CMOS device takes place in a single step and with a single mask, and that the silicide layer is deposited without further masking using selective CVD. Claim 17 is allowable as amended because the applied art requires multiple implantation and masking steps.

Claims 18-20 and 22 are allowable with their allowable parent claim.

In light of the foregoing amendment and remarks, the Examiner is respectfully requested to reconsider the rejections and objections stated in the Office action, and pass the

application to allowance. If the Examiner has any questions regarding the amendment or remarks, the Examiner is invited to contact the undersigned.

Respectfully submitted,

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